AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of performing memory mapped input output operations to an alternate address space comprising:

establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with a resource address designation having a plurality of fields of varying bit sizes with respect to one another, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said resource address designation; and

wherein a process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space.

2. (original) The method of Claim 1 wherein said first alternate address space is not a partition of a main address space from which said issuing process is executing.

3. (previously presented) The method of Claim 1 wherein said process issuing said at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space operates in a problem state of a machine.

4. (previously presented) The method of Claim 1 wherein said execution includes said at least one of said store and load with an allocated resources associated first alternate address space.

5. (previously presented) The method of Claim 1 wherein said problem state corresponds to a least privileged execution state.

6. (previously presented) The method of Claim 1 wherein said first alternate address space is associated with an adapter.

7. (original) The method of Claim 1 wherein at least one of said first instruction and said second instruction is executed without supervisory state intervention.

8. (cancelled)

9. (previously presented) The method of Claim 1 further including a second alternate address space associated with a second adapter.

10. (original) The method of Claim 9 wherein a storage location in said first alternate address space maps to a different address than the same location in said second alternate address space.

11. (original) The method of Claim 1 wherein said adapter includes address spaces as partitions of said alternate address space.

12. (original) The method of Claim 11 wherein said multiple address spaces are governed by at least one of a resource type and storage area types associated with said adapter.

13. (currently amended) A method of performing memory mapped input output operations to an alternate address space comprising:

establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store in accordance with a

resource address designation having a plurality of fields of varying bit sizes with respect to one another, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said resource address designation; and

wherein a process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space and operates in a problem state of a machine.

14. (previously presented) The method of Claim 13 wherein said problem state corresponds to a least privileged execution state.

15. (cancelled)

16. (original) The method of Claim 13 further including a second alternate address space associated with a second adapter.

17. (previously presented) The method of Claim 16 wherein a storage location in said first alternate address space maps to a different address than the same location in said second alternate address space.

18. (previously presented) A storage medium encoded with a machine-readable computer program code, said code including instructions for causing a computer to implement a method of performing memory mapped input output operations to an alternate address space, the method comprising:

establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with

a resource address designation having a plurality of fields of varying bit sizes with respect to one another, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said resource address designation; and

wherein a process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space.

19. (currently amended) A system for performing memory mapped input output operations to an alternate address space comprising:

a means for establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with a resource address designation having a plurality of fields of varying bit sizes with respect to one another, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

a means for establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said definition(s) of resource address designation; and

wherein a process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space.

20. (new) The method of claim 1 wherein the plurality of resource address designation fields further comprises:

an adapter identifier (AID) field, the AID field configured to designate the adapter;

a resource type (RT) field, the RT field configured to determine a particular class of resource from a possible set of resources of the adapter;

a resource identifier (RID) field, the RID field configured to determine a particular resource from a given resource type;

a storage area type (SAT) field, the SAT field configured to determine a particular class of resource storage from the possible set of resources of the adapter; and

a storage area offset (SAO) field, the SAO field configured to determine a byte offset within a given storage area type.

21. (new) The method of claim 13 wherein the plurality of resource address designation fields further comprises:

an adapter identifier (AID) field, the AID field configured to designate the adapter;

a resource type (RT) field, the RT field configured to determine a particular class of resource from a possible set of resources of the adapter;

a resource identifier (RID) field, the RID field configured to determine a particular resource from a given resource type;

.a storage area type (SAT) field, the SAT field configured to determine a particular class of resource storage from the possible set of resources of the adapter; and

a storage area offset (SAO) field, the SAO field configured to determine a byte offset within a given storage area type.

22. (new) The storage medium of claim 18 wherein the plurality of resource address designation fields further comprises:

an adapter identifier (AID) field, the AID field configured to designate the

adapter;

a resource type (RT) field, the RT field configured to determine a particular class of resource from a possible set of resources of the adapter;

a resource identifier (RID) field, the RID field configured to determine a particular resource from a given resource type;

a storage area type (SAT) field, the SAT field configured to determine a particular class of resource storage from the possible set of resources of the adapter; and

a storage area offset (SAO) field, the SAO field configured to determine a byte offset within a given storage area type.

23. (new) The system of claim 19 wherein the plurality of resource address designation fields further comprises:

an adapter identifier (AID) field, the AID field configured to designate the adapter;

a resource type (RT) field, the RT field configured to determine a particular class of resource from a possible set of resources of the adapter;

a resource identifier (RID) field, the RID field configured to determine a particular resource from a given resource type;

a storage area type (SAT) field, the SAT field configured to determine a particular class of resource storage from the possible set of resources of the adapter; and

a storage area offset (SAO) field, the SAO field configured to determine a byte offset within a given storage area type.